California DREAMS Cleanroom Gateway Handbook
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Introduction

This program enables any cleanroom facility to teach students with no prior semiconductor/microfabrication knowledge about a cleanroom experience. Students follow a process flow to manufacture a device. Along the way, they spend time with various critical tools, with three hours on a piece of equipment constituting enough exposure to earn a set of microcredentials from IEEE. Importantly, the students can earn these credentials in small blocks, such that they are “stackable”. Completion enables students to place IEEE badges for their LinkedIn profiles and, importantly, on their résumés.

The Gateway provides hands-on training in cleanrooms, in part because industry experts generally consider virtual training on fabrication steps unsuitable for in-person work. Every

program module (i.e., the work to earn each microcredential) combines short introductory sessions (labeled "Background" in Table 1) with cleanroom instruction where a qualified instructor demonstrates use of key equipment or carries out a specific process step. Subsequently each participant performs the same task under supervision. To ensure knowledge and skill retention, a good process visits every key equipment multiple times on different days. Learning is also reinforced by participants observing each other and receiving feedback from the instructor.

Consequently, the Gateway emphasizes short introductions and demonstrations, followed by participants using equipment under supervision. These sessions are not designed to create expertise but instead simply represent an initial exposure. As a result, all the microcredentials are labeled as an "introduction to X" (for fabrication step X) for hands-on introductions, or "fundamentals of X" for more in-depth hands-on components.

Course origin

The Cleanroom Gateway was developed by the University of Southern California (USC) and the University of California Santa Barbara (UCSB) and Santa Barbara City College (SBCC), with funding from the Department of Defense Microelectronics Commons to California Defense Ready Electronics and Microdevices Superhub (CA DREAMS) and from the National Science Foundation Advanced Technological Education (NSF-ATE) Program. Under DREAMS, the gateway was ported to USC from UCSB. UCSB has enjoyed great success in placing students in internships and full-time semiconductor jobs. UCSB had started running such 1-week bootcamps since 2022 via UCSB's Continuing Education and CNSI departments, in a close partnership with Santa Barbara City College (Dean Jens Kuhn); SBCC were the PI's on a 2021 NSF-ATE funded grant to develop the program with UCSB, and this program was ported to USC in 2024. The concept of training non-university participants in 1-week "boot camps" at university cleanroom facilities was disseminated from the NSF-ATE Centers SCME at the University of New Mexico (Prof. Matt Pliel) who also provided training, materials and fabrication processes; and CNEU/NACK at Penn State (Dr. Bob Ehrmann), in collaboration with the national ATE center MNT-EC (Prof. Jared Ashcroft). This handbook was inspired by Penn State's NACK Handbook.

Cleanroom safety and protocols

Industry experts agree that the ability to independently follow cleanroom safety and protocols is key to further training via follow-on internships and apprenticeships, and ultimately employment. Hence, our modules on safety and protocols are more extensive and the associated microcredentials are labeled as "Fundamentals of *Y*." They require higher levels of

instruction, formal quizzes, and extensive observation to ensure a safe environment for everyone.

Moreover, the safety microcredential includes safety instructions to be embedded in each fabrication step's instruction module. The instructor must ensure that each participant follows these practices. Likewise, the protocols' microcredential requires an understanding of a traveler/process follower/similar MES and requires participants to document their fabrication steps and the results of measurements for validation.

Consequently, the modules for individual fabrication steps contribute to the completion of the safety and protocols modules. Moreover, participants watching each other execute tasks earn time toward their protocols microcredential as well.

Course length

The level of learning must be calibrated to the program length. One week of 8 hour days (~40hr total) is sufficient to introduce students to a complete set of core steps/processes in semiconductor fabrication. The same content can optionally be performed over 2 weeks (10 days of 4-hr days) - some participant types prefer this. Notably, additional education, training, internship, or apprenticeship is required for full independence in a cleanroom.

Participant types

The Gateway serves three types of participants, all served within a single training cohort:

- S*tudents*, such as those enrolled in AS, BS or MS programs in relevant fields (e.g., Applied Physics, Chemical Engineering, Chemistry, Electrical and Computer Engineering, Materials Science, Mechanical Engineering, or Physics). Participants do not need prior background in semiconductors. In fact, we expect rising sophomores and recent transfers to BS programs to constitute a large percentage of our student cohorts.
- *Specialized learners*, i.e., adults with diverse education and work experience (e.g., automotive, manufacturing, etc.) who are exploring reskilling/upskilling via training and employment in the semiconductor sector.
- *New Gateway instructors,* such as technical staff from university cleanrooms. Instructor candidates should have a Master's degree or higher in a relevant field, 3+ years of industry experience. Gateway instructor candidates should have deep knowledge of the key fabrication steps, as well as cleanroom safety and protocols. Typically they have a role at a university cleanroom with responsibilities such as: fabricating devices for faculty and industry customers; and guiding/training graduate students, researchers, and

industry professionals who use their cleanrooms. During the training they observe experienced instructors deliver content and demonstrate equipment/process steps. Importantly, they observe how to support participants in hands-on work. Instructor candidates have one-on-one meetings with the instructor to seek clarifications and deepen their understanding of the vision and mechanics of executing a training program.

Participant outcomes

Gateway objectives vary with each participant type:

- *Students*: The Gateway introduces students to the skills, knowledge, and careers in semiconductors, as well as the impact of the semiconductor sector on society. The goal is to motivate them to pursue further education, research, and careers in semiconductors.
- *Specialized learners*: The Gateway helps them determine whether they are interested in careers in semiconductors and to make them attractive candidates for internships / apprenticeships in the industry. In-person experience for ≥1 week enables the participant to decide whether this industry suits them. A participant deciding that this industry is *not* of interest after the experience is also a useful outcome, both for the student and industry.
- *New Gateway instructors*: The Gateway accelerates their WFD program development by modeling and sharing key educational aspects of the program - namely, curriculum, pedagogy, and assessment. These participants also learn key considerations about the planning and logistics (e.g., materials purchases, development of a relevant process flow); and best practices in recruiting candidates and executing a program.

Learning modules

Table 1 describes the modules approved at the time of this document: Fundamentals of Cleanroom Safety (FCS) and Fundamentals of Cleanroom Protocols (FCP); and Introductions to Lithography, Deposition, Etching, and Metrology. For each module, Table 1 describes:

- Minimum instructional time outside the cleanroom.
- Minimum cleanroom time for instructor demonstration of the equipment/process and participant hands-on work (under instructor supervision).
- Safety and protocol training earned for each Introduction module.
- Expected learning outcomes.
- IEEE-compliant assessment method.

Assessments and badges

This syllabus is designed for compliance with IEEE processes and standards. Completion of a module enables the student to earn a microcredential, for which IEEE will issue a badge that can be showcased on resumes and LinkedIn.

Example assessments for completing the FCS and FCP microcredentials are available from USC and UCSB. An example answer key for USC's quiz can be found here. These are just example quizzes. Each cleanroom should administer quizzes that meet their own equipment and practices while conforming to the requirements in Table 1.

Assessments for other credentials have been built into the Fabrication Process Travelers that participants are already filling out during their Gateway cohort, since the assessments are for hands-on activities. For example, a single line added to the Traveler at the completion of the 2nd lithography step states:

Completion of Lithography with Alignment **Instructor Initials:_____**

The in-lab TA's can simply initial this line to indicate completion of this particular hands-on component of a microcredential. At least one such line should be initialled for each microcredential.

Research survey

California DREAMS is conducting a research survey in conjunction with this course. This research program is the Survey on Upgrading Cleanroom Competencies and Expertise in Semiconductor Skills (SUCCESS).

Use of this course material requires that you give students time to take the survey on Day 1 and on the last day – it should take 30 minutes in each session. You will receive the survey link from California DREAMS study personnel.

IEEE Microcredentials: Topics and Requirements

The following table lists each IEEE Microcredential developed by the CA DREAMS Hub, along with (a) the content that should have been covered in the gateway to achieve the credential, and (b) the minimum number of hours + days spent in-class to achieve each.

Hours spent in the lab can contribute to *multiple* credentials simultaneously; for example, the participant is accruing "Fund. of Cleanroom Protocols (FCP)" (wearing/utilizing cleanroom gowns & tools), "Fund. of Cleanroom Safety (FCS)" (safe chemical usage), and "Intro. to Lithography" (using lithography tools) simultaneously, when they are performing a lithography step, since all of these skills are utilized/learned at the same time.

Table 1: IEEE Microcredential Fulfillment Requirements

	Audience	Introduction to Lithography	Introduction to Deposition	Introduction to Etching	Introduction to Metrology	Fundamentals of Cleanroom Safety (FCS)	Fundamentals of Cleanroom Protocols (FCP)	Gateway instructor
Description		Under supervision, performed spin-coating and curing of photoresist on wafer. Aligned, exposed and developed a pattern using Contact Aligner or similar tool.	Observed and participated in deposition of metal or dielectric onto product wafers according to work instructions. Participated in patterning of deposited layers.	Observed and participated in wet and dry etch to transfer lithography pattern to wafer.	Under supervision, used profilometer to measure and record the thickness of patterned materials. Used microscope to inspect for defects, and measure + record dimensions of patterns on wafer.Used optical techniques to measure and record thickness of thin-films on-wafer.	Learned and followed cleanroom emergency procedures - PPE, chemical storage/disposal, eye wash/shower, spill kits, gas/fire alarms. Intro. to material safety data sheets (MSDS) and chemical and gas hazards. Safely utilized chemicals such as solvents, developer, water, glassware and chemical benches/fume hoods.	Followed cleanroom protocols: wearing Personal Protective Equipment (PPE), cleanroom gowning procedures, wafer handling with tweezers/dippers, work space/equipment cleanliness. Utilized production MES systems such as traveler / runcard / work instructions and recording. Used different types of benches/fume hoods for different chemicals and followed multiple equipment standard operating procedures (SOP). Introduction to cleanroom classes, materials restrictions and cleaving wafers.	
Background (Note-1): Min hours	STLs, SPLs, ICs	1	1	1	1	2	2	
Cleanroom work (Note-1): Min hours	STLs, SPLs, ICs	2	2	2	2	8 (Note-2, Note-3)	8 (Note-2, Note-3)	

Min days		1	1	1	1	3	3	4
Concurrently contributes to		2 hours to FCS & 2 hours to FCP	2 hours to FCS & 2 hours to FCP	2 hours to FCS & 2 hours to FCP	2 hours to FCS & 2 hours to FCP			
Debriefing for the ICs (Note-1): Min hours	ICs	0.5	0.5	0.5	0.5	0.5	0.5	
Learning Outcomes: STLs & SPLs should be able to....		Perform lithography under supervision	Perform deposition under supervision	Perform etching under supervision	Perform metrology under supervision	Learn and then independently follow cleanroom safety practices.	Learn and then independently follow cleanroom protocols such as following work instructions and SOPs. Record and communicate observations during process (eg. via traveler / follower / runcard / MES).	
Learning Outcome: ICs should be able to....		Provide or supervise training on lithography.	Provide or supervise training on deposition.	Provide or supervise training on etching.	Provide or supervise training on metrology.	Provide or supervise training on cleanroom safety.	Provide or supervise training on cleanroom protocols.	
Assessment Method for STLs & SPLs #1		A qualified instructor observed the learner successfully completing the task.	A qualified instructor observed the learner successfully completing the task.	A qualified instructor observed the learner successfully completing the task.	A qualified instructor observed the learner successfully completing the task.	A qualified instructor observed the learner successfully completing the task.	A qualified instructor observed the learner successfully completing the task.	
Assessment Method for STLs & SPLs #2						Quiz on Safety protocols, >80% score (multiple submissions allowed, open-book) (Note-4)	Quiz on Safety protocols, >80% score (multiple submissions allowed, open-book) (Note-4)	
Assessment Method for ICs		A qualified instructor assessed, via one-on-one discussions, the instructor candidate's understanding of the selection of topics and skills to cover, pedagogical methods, and the process of assessing student/specialized learners.						

	Student learners: **STLs**	Specialized learners: **SPLs**	Instructor candidates: **ICs**		
Note-1	Cleanroom hours include hands-on work; hours in the table minimum per student.				
	Minimum hours required to complete all six micro-credentials is 16. However, each program's hours can be higher (e.g. the USC total program time is 35 hours of which 27 hours are spent in the cleanroom).				
	Some of the cleanroom hours are the time when a learner observes other learners working and receiving feedback from the instructor.				
Note-2	Some of the observation of cleanroom protocol is the time when a learner observes other learners working and receiving feedback from the instructor.				
Note-3	The microcredentials for individual fabrication steps also contribute to the FCS and FCP microcredentials (see table row entitled "Concurrently contributes to")				
Note-4	Examples of FCS and FCP quizzes can be found at this link.				

Coordinator

California DREAMS has a coordinator who assists in the maintenance of records for our research and for implementation of the credential program. Once you have set a date and prepared an application for your cohort, you will provide that information to the coordinator, Charles Parker (charlesp@usc.edu), and he will ensure it is public on our website, https://dreamsgold.org/ , for anyone interested to view and apply.

Once the cohort has been selected, you will send their information to the coordinator. Once the program is over, you will deliver a roster of completed assessments. The coordinator will then upload to IEEE, who will issue the badges to student's emails.

For institutions participating in the Cleanroom Gateway, the following steps provide a detailed outline of responsibilities and processes. These ensure a seamless execution of the credential program while maintaining consistency across all locations. Institutions should follow these steps closely in collaboration with the program coordinator:

1. Institution applies to IEEE to get approval to teach the course https://www.ieee.org/education/credentialing/index.html
2. Institution develops its program based on the Handbook, receives approval from IEEE.
3. Institution sets the date for the cohort.
4. Institution shares its plan with the Coordinator. This should include the schedule, projects cohort will work on, and information on any trainers or instructors for the program.
5. Institution prepares and distributes the application.
6. Institution selects cohort.
7. Institution shares cohort information with the coordinator.
8. Coordinator adds cohort to Master Spreadsheet for tracking research and credential implementation.
9. Program begins.
10. On the first day, the instructor distributes the research survey.
11. Instructor oversees IEEE evaluation forms & assessment at the end of each module.
12. On the last day, the instructor distributes the research survey.
13. Program wraps.
14. Within 1 week, the instructor delivers to the Coordinator a roster of completed assessments.
15. Coordinator uploads the roster of completed assessments and evaluations to IEEE.

16. IEEE issues credentials/badges and invoices. Invoices must be paid by the institutions who delivered the training. The cost for every microcredential issued by IEEE is $25. For more information, contact Christine Cherevko, Program Specialist c.cherevko@ieee.org.

Train the Trainer

The Cleanroom Gateway is designed to train new Gateway instructor candidates. To train a candidate, a facility must:

- Submit a candidate CV to the Gateway leadership at California DREAMS.
- Send the candidate to a Gateway course for participation in all sessions, as well as one-on-one sessions with the instructor.

When the Gateway instructor approves of the candidate, the name will be added to the Gateway roster.

Key takeaways/insights for running your own gateway

- The purpose of a "gateway" training is not to produce experts, but instead to provide an experience for interested participants to continue into the industry if desired. Hands-on, in-person experience is critical to enable participants to make that decision. Participants that decide *not* to pursue the semiconductor industry are also useful outcomes - some often go into adjacent "precision manufacturing" careers, such as aerospace or biomedical.
- Keep the gateway as short and simple as possible while still meeting the necessary requirements. This (a) allows you to run it more often if it is ≤2-weeks long, and (b) reduces participant fatigue while still performing the intended gateway function.
- Avoid complex engineering-level explanations when not needed. This avoids discouraging sub-university students from participating, who may erroneously think that only higher-education levels can work in the semiconductor industry.
  Almost no math is needed in a gateway course (at most *rate = thickness x time*), as this is a one-week introduction only.
  - Choosing what *not* to teach/say is arguably more important than what to include, especially when taught by fabrication experts.
  - Students can learn the complexities in later courses if they choose to continue.
  - The gateway often reveals to participants for the first time that sub-PhD education can still result in gainful semiconductor employment.
- Industry have indicated that the utility of a 1-week gateway reduces their risk as follows:

- Identify participants that can work in the manufacturing environment, will wear PPE, follow protocols and operating procedures, and follow safety protocols; for whom the cleanroom environment is not a deterrent.
- Identify participants that are “trainable”, and have excitement to learn more. They do not have to be fully “trained”.
- Industry will train new-hires on their own processes - your training does not need to (and can not) train on one company’s specific fabrication process.
- Identify participants that have the dexterity and attention to detail required for microfabrication-level wafer handling. Participants may often take jobs adjacent to microfab - such as testing, assembly, machining etc. within semiconductor/precision manufacturing companies.
- Preventing a participant from applying for a job they would not enjoy is an extremely valuable outcome of a gateway course. (One industry partner referred to this as a “filtering function” of the cleanroom gateway.)

Authors

Demis D. John (UC Santa Barbara, Nanofab); Andrea Belz, Shiva Bhaskaran, Sandeep Gupta, and Rehan Kapadia (USC); and Christine Cherevko and Jennifer Fong (IEEE). Thanks to Dean Jens Kuhn (Santa Barbara City College).

Appendix A: Sample Schedules used by UCSB and USC in Summer 2024

These are example schedules from gateways at UCSB and USC. Both of these offerings cover all the proposed requirements and exceed the minimum numbers of required hours in Table 1. Further, in Summer 2024 USC offered training that spanned two weeks. However, all USC's future offerings will use a format similar to the USCB schedule below, starting on Monday mornings and ending on Fridays at noon. Each cleanroom should develop a schedule that meets their equipment and practices while conforming to the requirements in Table 1.

UCSB 1-Week Cleanroom Gateway Program (8/12/2024 - 8/16/2024)

LUNCH break will be 12:00 PM - 1:00 PM, daily, except on 8/15

DAY	TIME	IN CLASSROOM (ELINGS 3001)	TIME	IN CLEANROOM
8/12	9:00 AM - 12:00 PM	Industry Introduction Cleanroom & Gowning & PPE Semiconductor Basics part 1: Substrates and Photolithography Units Art Wafer and Traveler Outside Tour - facilities	1:00 PM - 5:00 PM	Gowning practice & Safety Review Art Wafer Pt. 1
8/13	9:00 AM - 10:00 AM	Semiconductor Basics part 2: Deposition/Etching Introduction to Vacuum Systems	10:00 AM - 12:00 PM	Art Wafer Pt. 2 Etch + Strip
	1:00 PM - 2:00 PM	Course alumni presentation Pressure sensor explain and process flow	2:00 PM - 5:00 PM	Make Pressure Sensor Pt. 1 Metal Litho + Evap (+passdown)
8/14	9:00 AM - 10:00 AM	Wafer Handling/Passdown/Automated Travelers/Recording +Reporting Observations	10:00 AM - 12:00 PM	Make Pressure Sensor Pt. 2 Liftoff + µScope Meas
	-	-	1:00 PM - 5:00 PM	Make Pressure Sensor Pt. 3 BS Litho: Spin+Exp+Dev
8/15	9:00 AM - 10:00 AM	Metrology Pressure Sensor Process Update	10:00 AM - 12:30 PM	Make Pressure Sensor Pt. 4 In Nanofab: RIE SiN Etch (2 batches) In CNSI: PR Strip, KOH Insert
	2:00 PM - 3:00 PM	Electrostatic discharge (ESD) / Statistical Process Control	3:00 PM - 5:00 PM	Make Pressure Sensor Pt. 5 Metrology Training (Dektak, Filmetrics, µScope) KOH (already inserted)
8/16	9:00 AM - 10:00 AM	Recap basic process steps: Litho/Dep/Etch	10:00 AM - 12:00 PM	Post-KOH Inspection/meas, Cleaving Demos/Tours: - 5x CNSI SEM - 5x CNSI Microfluidics Lab
	2:00 PM - 4:00 PM	Interviews - Program Evaluation	-	-

USC 2-Week Cleanroom Gateway Program (6/3/2024 - 6/14/2024)

LUNCH break will be 12:00 PM - 1:00 PM, daily, except on 6/13

Team MEET at MCB Lobby daily at 9:30am

DAY	TIME	TOPIC	LOCATION
6/3	10:00 AM - 11:00 AM	Cleanroom lecture	MCB Conference room 102
	11:00 AM - 12:00 PM	Cleanroom Facility, Ist floor gas system ,TGMS, Emergency meet location, window tour	MCB Building
	1:00 PM - 1:30 PM	Cleanroom Gowning procedure/ Gown reservation	MCB Lobby
	1:30 PM - 2: 30 PM	Cleanroom orientation	Cleanroom Room #LL103
		Participant finish Cleanroom quiz online	
6/4	9:30 AM - 10:30 AM	Wafer Cleaving/Handling/Photolithography lecture	MCB Conference room
	10:30 AM - 12:00 PM	Wafer Handling/Wafer Cleaning/Photolithography	Cleanroom Room #LL103
	1:00 PM - 3:00 PM	Wafer Handling/Wafer Cleaning/Photolithography	Cleanroom Room #LL103
6/5	9:30 AM - 10:30 AM	MEMS/BioMEMS lecture	MCB Lobby
	10:30 AM - 12:00 PM	Art wafer Photolitho	MCB Conference room
	1:00 PM - 3:00 PM	Art wafer /Metal Deposition/Lift off	Cleanroom Room #LL103
6/6	9:30 AM - 10:30 AM	Deposition Lecture	MCB Conference room
	10:30 AM - 11:00 AM	Lift off	Cleanroom Room #LL103
	11:00 AM - 12:00 PM	F20 Thickness measurement/ Dektak	Cleanroom Room #LL103
	1:00 PM - 2:30 PM	Sputtering/EBeam Evap/ALD	
6/7	9:30 AM - 10:30 AM	Etching Lecture	MCB Conference room
	10:30 AM - 11:30 AM	Heidelberg DWL 66+ Group1	Cleanroom Room #LL103
	11:30 AM - 12:00 PM	Traveler - Wafer cleaning/Spinner/Photolitho/Dektak Group2	
	12:30 PM - 1:30 PM	Traveler - Wafer cleaning/Spinner/Photolitho/Dektak Group2	Cleanroom Room #LL103
	1:00 PM - 2:00 PM	Heidelberg DWL 66+ Group1	Cleanroom Room #LL103
6/10	10:00 AM - 11:00 AM	Wafer scribe Group1	Cleanroom Room #LL103
	10:00 AM - 11:00 AM	Desktop SEM Group1	Cleanroom Room #LL103
	11:00 AM - 12:00 PM	Wafer scribe Group2	Cleanroom Room #LL103
	11:00 AM - 12:00 PM	Desktop SEM Group2	Cleanroom Room #LL103
	1:00 PM - 2:00 PM	Etch Group1	Cleanroom Room #LL103

	1:00 PM - 2:00 PM	Neural Probe - 1st PI spin coat and curing Group2	Cleanroom Room #LL103
	2:00 PM - 3:00 PM	Etch Group2	Cleanroom Room #LL103
	2:00 PM - 3:00 PM	Neural Probe - 1st PI spin coat and curing Group1	Cleanroom Room #LL103
6/11	10:00 AM - 12:00 PM	Neural Probe - 1st layer Photoresists/Photolitho	MCB Lobby
	1:00 PM - 2:30 PM	Neural Probe Metal deposition/Lift off	Cleanroom Room #LL103
	2:30 PM - 3:00 PM	Etch Traveller Staff Demo (Joey arrange time with the group for next day)	Cleanroom Room #LL103
6/12	10:00 AM - 12:00 PM	Etch Traveller - Ellipsometer	Cleanroom Room #LL103
	1:00 PM - 2:30 PM	Etch Traveller - Dektak	Cleanroom Room #LL103
	2:30 PM - 3:30 PM	Neural Probe- 2nd PI Spincoat and curing	Cleanroom Room #LL103
6/13	9:30 AM - 10:30 AM	MEMS/Packaging Lecture	MCB Conference room
	10:30 AM - 11:30 AM	Neural Probe - 2nd Photoresists/Photolithography Alignment Group 1	Cleanroom Room #LL103
	10:30 AM - 11:30 AM	Wire Bonding Group 1	Cleanroom Room #LL103
	12:30 PM - 1:30 PM	Neural Probe - 2nd Photoresists/Photolithography Alignment Group 2	Cleanroom Room #LL103
	12:30 PM - 1:30 PM	Wire Bonding Group 2	Cleanroom Room #LL103
	1:30 PM - 3:30 PM	DRIE Etching 1, 2, 3	Cleanroom Room #LL103
6/14	9:30 AM - 12:00 PM	DRIE Etching 4,5,6,7	Cleanroom Room #LL103
	1:00 PM - 1:30 PM	CNI Tour	
	1:30 PM - 2:30 PM	CNI - SEM	
	2:30 PM - 3:00 PM	SMRL Tour	
	3:00 PM - 4:30 PM	Evaluation & Internship plans	MCB Conference room

Appendix B: Sample Projects used by UCSB and USC in Summer 2024

These are sample projects that each learner completed during the hands-on in-cleanroom part of their training. Each cleanroom is welcome to use these prior projects or create their own (to match their equipment), but the level of participant difficulty and the work required must fit within the cleanroom hours offered for each microcredential. DREAMS Staff can assist in helping you tailor your fab's projects. You can find more information at Link 1 and Link 2.

B.1) UCSB/SBCC Project: Pressure Sensor

B.2) UCSB/SBCC Project: Art Wafer (Demo Product)

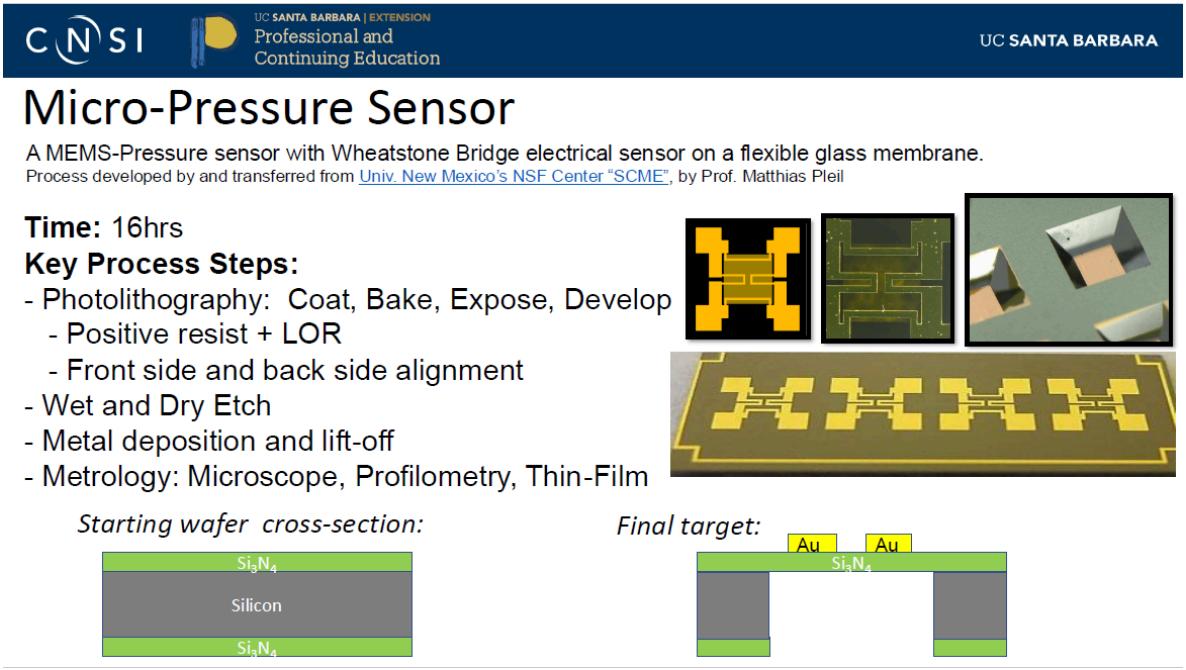
B.3) USC Project: Microfabrication of Polyimide Microelectrode Arrays and Art Wafer

B.4) USC Project: Micro-Pressure Sensor

UCSB/SBCC Project: Pressure Sensor

The Micro-Pressure Sensor, originally developed by Prof. Matt Pliel at UNM, is a two-layer process with 2 lithographies, one on the front for metallization and one on the backside for KOH through-wafer etch, resulting in a suspended SiN membrane.

UCSB added additional industry-relevant components, such as a night-shift passdown, in which lab Teaching Assistants run the metal evaporation in the evening and "pass-down" the steps performed via an email report to participants, who then continue the process the next day.



Full Traveler (google sheets) can be downloaded here.

UCSB SBCC	PRESSURE SENSOR		Rev. 2024-08-11			Tracking Initials/Date	
	Procedure	**Materials**	**Machine / Bench**	**Program / Rcp.**	**Parameters**	**Details on Step**	W1	W2
	Initial Wafers							
	Silicon wafers, 3-inch diameter, single-side polished, with 1000nm SiN coating on both sides. Starting Si-wafer thickness is 380 um.							
	Frontside Wheatstone Metal Resistors							
	Frontside Wheatstone Bridge Patterning							
1	YES - O2 plasma		YES R3 Plasma Asher	Program #1 (1min) 300W Bottom Rack	Program #1 (on black dial) Bottom rack. Do not use the top rack. If reworking old wafer, use top rack and program #3.	When plasma lights (after ~2min), turn "level" knob to set Power to "0.300 kW"		
2	HMDS Primer Spin	HMDS	Solvent bench spinner	3 KHMDS 10sec soak, program recipe A	3000 RPM	Center wafer on chuck, engage vacuum. Have to turn on both the VAC and CDA. Pipette HMDS on wafer (cover 1/2-2/3 of wafer), start program.		
3	HMDS Primer Bake		Solvent bench spinner		100°C - 60s			
4	Cool down		Grating next to hotplate		1min			
5	AZ 1518 Coat	AZ 1518	CEE Coat/Bake	1518 2,5K_CC-PRIME	2500 RPM (60s)	Place the wafer on the spin chuck and then center then wafer. Once the wafer is centered, dispense resist until 50% of the wafer surface is covered, close the lid and start the spin program. When the program ends, open the lid of the CEE Coater, remove the wafer and place it on the hot plate.		
6	Soft Bake		CEE Coat/Bake	100C	100°C - 60 s	When baking is complete, remove the wafer and place on the table to cool. Two tweezers may be needed.		
7	Cool down		Grating next to hotplate					
8	**Photoresist Spin Completed (Intro to Litho.): Instructor Initials**							
10	***Frontside "Metal" layer Expose***							
11	Setup Exposure		Karl Suss MA6	Make sure the lamp is set to Ch 1.	Mask Title: UCSB_CNSI_MPS_v7 Layer: Topside_Metal Version: v7, 2022-07-27 (Demis D. John) 4-inch wafer chuck	A 4-inch chuck works for 3-inch wafers. Place the mask in the mask holder and turn on the mask vacuum.		
10	Check lamp power		Karl Suss MA6			Record lamp power prior to first exposure. Adjust exposure time if need be to achieve the dose needed.		

13	Expose		Karl Suss MA6	Soft Contact* (note, this is different from Art Wafer)	Contact gap: 50 um Exposure Time: 9.3 sec (or adjust according to measured power) Wavelength: 365 nm Dose needed: 136 mJ/cm^2 Very tolerant	Select the program and set the parameters, including exposure time and soft contact mode. Coarsely align (by hand) wafer to marker line prior to exposure. Soft contact ensures that the wafer won't stick to the mask plate. To move the MA6 microscope head down, press F1 + down + enter.		
14	Post Exposure Bake (PEB)		Hot Plate		100°C - 90 seconds	The PEB is used to diffuse the exposed and unexposed photoactive compound (PAC) and smooth out any standing wave effects in the photoresist.		
15	Cool down		Grating next to hotplate		1min			
16	Develop	AZ300MiF	Developer Wet Bench		60 s	Develop with gentle agitation for 60sec.		
17	Rinse #1	DI Water	Developer Wet Bench			Transfer into another beaker with DI water. This waste gets collected in a container.		
18	Rinse #2	DI Water	Developer Wet Bench			Second, rinse in the final bucket before drying. This waste can go down the drain.		
19	N2 Dry		Developer Wet Bench			N2 gun dry on cleanroom wipe		
20	Develop Inspect		Microscope			Check to make sure the resist has cleared - should be a single uniform color everywhere. If you see rainbow colors, then resist is not fully removed. Check that the features are well-defined and clean. If not, proceed to re-work the wafer.		
21	**Photolithography Completed (Intro to Litho.): Instructor Initials**							
22	***Re-working wafers, if necessary***							
23	ACE Rinse	ACE	Solvent Bench /Dish		~30sec	Rinse off any metal particles, using just enough solvent to cover the wafer Do NOT let Acetone dry on the wafer, will leave streaks		
24	IPA Rinse	IPA	Solvent Bench / Dish		~30sec	Use IPA Squirt Bottle as removing to ensure fresh IPA only		
25	N2 Dry		Solvent Bench			N2 gun dry on absorbent wipe		
26	YES - O2 plasma		YES R3 Plasma Asher	Program #3 (5min) 300W Top Rack	Make sure to use top rack and program #3 for reworking wafers	*When plasma lights (after ~2min), turn "level" knob to set Power to "0.300 kW"*		
27	Restart photoresist spin (line 2)							
28	***Metallization***							
29	***Night-Shift Passdown***					This step will be performed by the night shift. [Intro. Protocols] Make sure to fill in the tracking columns when you receive their passdown		
30	Metallization	Cr/Au	Nanofab EBeam #4 Back-up: EBeam #1		Cr: 30Å @ 1Å/sec Au: 1000Å @ 1-->5Å/sec	Use a 9 x 4-inch wafer holder. Mount 3-inch wafers with clips.		
32	***Metal Lift Off***							

33	Prepare Ultrasonic Bath	DI	Large Fisher Scientific Sonicator Solvent Bench - Crest Ultrasonic			Fisher Scientific Sonicator (large bath): fill with DI water. [ON] to begin Ultrasonication. CREST Ultrasonic: fill with DI water. Set power to level 8. [Sonics ON] to begin Ultrasonication		
34	Metal Lift-Off	Acetone	Large Fisher Scientific Sonicator, then Solvent Bench - Crest Ultrasonic		~2min on highest power, observe until clear. Make sure the edges are fully clear. Some light swabbing may be necessary.	Place wafers in a dish of FRESH acetone (avoid reusing), ~1-inch deep liquid or so. Place wafers (in dishes) in a large sonicator to begin the lift-off process. Press "on" to start sonication. The large sonicator sonicates more weakly. Move wafers (in dishes) one-by-one into the smaller, faster sonicators. Continue sonication until sufficient metal lift-off is achieved. When the time is over, rinse the wafer with a squirt bottle filled with acetone to remove some of the gold that might still adhere to the wafer. SWAB with cotton swab (not plastic) while submerged in ACE in sonicator. Do NOT let Acetone dry on the wafer, it will leave streaks.		
35	ACE Rinse	ACE	Solvent Bench / Dish		~30sec	Rinse off any metal particles Do NOT let Acetone dry on the wafer, it will leave streaks.		
36	IPA Rinse	IPA	Solvent Bench / Dish		~30sec	Use an IPA Squirt Bottle as removing to ensure fresh IPA only.		
37	N2 Dry		Solvent Bench			N2 gun dry on absorbent wipe		
38	Inspect		Microscope			Inspect the wafer(s) to make sure that the metal has lifted off around the wheatstone bridge circuit.		
39	IF metal particles are present on >25% of devices (eg. many devices are shorted/damaged) Redo from ACE-Sonicate-Swab step.				Go to Ultrasonic Bath again (line 30)	Repeat until ~75% of devices are clean of metal particles. Particles/defects in the unused open space are acceptable.		
40	**Deposition and Lift-Off Completed [Intro to Dep.]: Instructor Initials**							
41	Measure Metal Width		Leica Microscope			Measure Width of Metal traces on appropriate device. Place cursors on OUTSIDE of metal lines to get measurement.		
42			Leica Microscope		Measure feature: MW20 Metal Width	*[Intro. Metro.] Record Measurement:*		
43			Leica Microscope		Measure feature: MW150 Metal Width	*[Intro. Metro.] Record Measurement:*		
44	Save Microscope Pictures		Leica Microscope			Filenaming Scheme: <date>-<Initials>-<WaferNumber>-<MW20/MW150>-<ImageNumber>.jpg		
45	***Backside Membrane Window***							
46	***Frontside Coat***							

47	HMDS Primer Spin	HMDS	Solvent bench spinner	3KHMDS 10sec soak, program recipe A	3000 RPM	Center wafer on chuck, engage vacuum. Pipette HMDS on wafer (cover 1/2-2/3 of wafer), start program		
48	HMDS Primer Bake		Solvent bench spinner		100°C - 60s			
49	Resist Coat	AZ 1518	CEE Coat/Bake	**1518 1K CCPRIME **note that this is different from the Metal/front-side litho**	1000RPM *spin speed is slower	Place the wafer on the spin chuck and then center then wafer. Once the wafer is centered dispense 2ml of the resist, close the lid and start the spin program. When the program ends, open the lid of the CEE Coater, remove the wafer and place it on the hot plate. Spin speed is slower to make the resist thicker to stand up to etching down the road		
50	Soft Bake		CEE Coat/Bake		100°C - 2 min	When baking is complete, remove the wafer and place on the table to cool.		
51	Cool down		Grating next to hotplate					
52	***Backside Coat***							
53	HMDS Primer Spin	HMDS	CEE Coat/Bake	3K HMDS 10sec soak	3000 RPM	Center wafer on chuck, engage vacuum. Pipette HMDS on wafer (cover 1/2-2/3 of wafer), start program.		
54	HMDS Primer Bake		CEE Coat/Bake		100°C - 60s			
55	Resist Coat	AZ 1518	CEE Coat/Bake	1518 1K CCPRIME	1000RPM	Place the wafer on the spin chuck and then center then wafer. Once the wafer is centered dispense 2ml of the resist, close the lid and start the spin program. When the program ends, open the lid of the CEE Coater, remove the wafer and place it on the hot plate.		
56	Soft Bake		CEE Coat/Bake		100°C - 2 min	When baking is complete, remove the wafer and place on the table to cool.		
57	***Backside Expose - Membrane Mask***							
58	Setup Exposure		Karl Suss MA6		Mask Title: UCSB_CNSI_MPS Layer: Backside_KOH Version: v9, 2022-07-27 (Demis D. John) 4-inch wafer chuck	4-inch chuck works for 3-inch wafers but loses vacuum. Place the mask in the mask holder and turn on the mask vacuum. Will show "Loss of Wafer Vacuum" during load - [Enter] to continue		
51	Check lamp power		Karl Suss MA6			Record lamp power prior to first exposure. Adjust exposure time if need be to achieve the dose needed. Record Lamp Power -->	Lamp Power:	

60	Expose		Karl Suss MA6	Soft Contact	Contact gap: 50 um Exposure Time: 59.5 sec Adjust for measured power: _____ Wavelength: 365 nm Dose needed: 550 mJ/cm^2 Time = Power / Time	Backside alignment procedure. [Top Bottom] Lit (backside camera control) Check camera location with no plate or wafer inserted. Should line up with Arrows on the mask plate. Have to [Grab Image] on the Mask Plate "Top Substrate" first, then [Load] wafer 2nd. From this point do not adjust the camera again with arrows, since it is in a good location. Move wafer with manual turn knobs, not arrows. Must [Grab Image] with no wafer each time between wafers.		
61	Develop	AZ300MiF	Developer Wet Bench		2 minutes			
62	Rinse #1	DI Water	Developer Wet Bench			This waste must be COLLECTED in container		
63	Rinse #2	DI Water	Developer Wet Bench			This waste may be poured down the SINK		
64	N2 Dry	N2 Gun	Developer Wet Bench					
65	Develop Inspect		Microscope			Check that areas exposed are cleared of resist. Develop again if necessary.		
66	**[Intro to Litho.]: What is the purpose of lithography? (Free-form answer):**							
67	***Nitride Etch (At Nanofab)***							
68	Plasma Etch	CF4/O2	NanoFab PEii Technics Asher #2	300mT / 250W	10 min - 300 mTorr, 250W	Cover platen with wafers (max five at a time). It's possible more wafers will lower etch rate a bit.		
69	Inspect		By Eye			Inspect to see if there is color in the KOH Window areas, should have some color variation in the holes		
70	Rotate wafers 180°					Rotating wafers helps with etch uniformity - etcher is slightly faster towards the middle of the chamber.		
71	Plasma Etch	CF4/O2	NanoFab PEii Technics Asher #2	300mT / 250W	10 min - 300 mTorr, 250W	Cover platen with wafers. It's possible more wafers will lower etch rate a bit.		
72	Etch Inspect		By Eye			Check to see if the nitride has been etched correctly. Should show uniform silicon-gray color in openings.		
73	Resist Strip	ACE	Solvent Bench		approx 1 min	Fill the flat beaker with acetone and place the wafer in for a minute. Don't let Acetone dry on the wafer, as before. Note: Sonication may be needed to remove backside PR.		
74	Rinse	IPA	Solvent Bench		~15-30 sec			
75	N2 Dry	N2	Solvent Bench / N2 Gun		On absorbent wipe	N2 gun dry		
76	**Dry-Etch Completed [Intro to Etch.]: Instructor Initials**							
77	**[Intro to Etch.]: What is the purpose of etching? (Free-form answer):**							

78	***Membrane Release***							
79	***Pressure Sensor Cavity Etch***							
80	Optional: Measure Depth		Dektak XT		Large Range ~65µm Measure into window prior to KOH etch	Record measurement -->		
81	Setup KOH bath	KOH	KOH Bath - Acid/Base Bench		90°C	Fill up the bath above the level of wafers in holders. Note bath level for later refilling to the same level. Turn on Nitrogen bubbler to "stir" solution, but GENTLY so it doesn't damage released membranes		
82	KOH Etch	KOH	KOH Bath - Acid/Base Bench		90°C - 4 hours (approx)	Etch wafer(s) in a solution that is 35% KOH. Cover with lid.	In= Out=	In= Out=
83	Rinse #1	DI Water	Water container		30sec	This waste must be collected in under-bench waste container		
84	Rinse #2	DI Water	Waterfall DI Water Rinse		1 minute full Drain below wafer level 1min full	Rinse using ONLY the bottom DI water inlet to prevent breaking the wafers.		
85	N2 Dry		Nitrogen Gun - Acid/Base Bench			Gently spray wafer dry using the nitrogen gun. Reduce N2 gun pressure!! Place wafer face-up on absorbent napkins.		
86	Measure Depth		Dektak XT		Large Range ~65µm Measure into KOH window	[Intro. Metro.] Record measurement -->		
87	Calculate KOH Etch Rate & Remaining Time				Starting Si wafer thickness: 380 µm	Rate = Etch Depth / Etch Time [Intro. Etch] Remaining Time to complete etch -->		
88	Refill KOH bath	KOH	KOH Bath - Acid/Base Bench		Refill with DI water up to same level as initial setup			
89	KOH Etch	KOH	KOH Bath - Acid/Base Bench		90°C - 4 hours	Continue etching.	In= Out=	In= Out=
90	Inspect		Microscope					
91	Rinse #1	DI Water	Water container		30sec	This waste must be collected in under-bench waste container		
92	Rinse #2	DI Water	Waterfall DI Water Rinse		1 minute full, then Drain to below wafer level, then 1min full	Rinse using ONLY the bottom DI water inlet to prevent breaking the membranes.		
93	N2 Dry	N2	Nitrogen Gun - Acid/Base Bench			Reduce N2 gun pressure!! Place wafer face-up on absorbent napkins. Gently dry using the nitrogen gun		
94	**Wet-Etch Completed [Intro to Etch.]: Instructor Initials**							
95	Optional: Measure Depth		Dektak XT		Large Range ~65µm Measure into KOH window	Record measurement -->		
96	Inspect		Microscope			Take photos.		
97	**Micro-Pressure Sensor Wafer Completed [Demo.]: Instructor Initials**							
98	Cleave product wf. or separate Si wf.							
99	**Wafer Cleaving Completed [Intro to Protocols]: Instructor Initials**							

UCSB/SBCC: Art Wafer (Demo Product)

The “Art Wafer”, originally developed by Prof. Matt Pliel @ UNM, is run on Day 1, to increase student engagement. Prior to attending the gateway, students upload/send an image/photo of their choice, which will be printed onto their Art Wafer using photolithography & etching. The fact that students will take this Art Wafer home dramatically increases their desire for success!

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Introduction: Art Wafer

Students provide a photo of their choice, which will be imprinted into the blue SiO2 layer on a silicon wafer.



Time: 8hrs

Key Process Steps:

- Photolithography: Coat, Bake, Expose, Develop
- Positive resist
- Wet Etch
- Metrology: Microscope, Step Height

Starting wafer cross-section:



Final Wafer:



Full Traveler (google sheets) can be downloaded here.

	UCSB	ART WAFER		rev. 2024-08-11			Wafers Run	
	IMPORTANT STEPS	**Chemicals**	**Machine/ Bench**	**Program/Recipe**	**Parameters**	**Details on Step**	**W1**	**W2**
1	***Exposure Prep: Check Lamp Power***							
2	Record lamp power (supervisor) Lamp power: *(mW/cm2*		Karl Suss MA6 Contact Aligner			*record lamp power in morning prior to wafer exposure (should be ~8.1 mW/cm2)*		
3	***Hexamethyldisilazane (HMDS) Deposition - spin coater***							
4	YES - O2 plasma		YES R3 Plasma Asher	Program #1 (1min) 300W Bottom Rack	Program #1 (on black dial) Bottom rack. Do not use the top rack. If reworking old wafer, use top rack and program #3 (5 min)	*When plasma lights (after ~2min), manually turn "level" knob to set Power to "0.300 kW"*		
5	HDMS Primer Spin	HMDS	WS-400BZ-6NPP LITE (Spinner #1 in solvent	3krpm, 60 sec, 130rpm/s, HMDS 10 sec soak before spinning (Recipe A)	Center wafer on chuck, engage vacuum Pipette HMDS on wafer (cover 1/2-2/3 of wafer), start program	*HMDS is hazardous to inhale, close lid of coater prior to spinning*		

			bench #2)					
6	HDMS Primer Bake		Thermo Hotplate on solvent bench		100°C for 90sec			
7	Cool down		Grating next to hotplate		1min			
8	***Photoresist Application - CEE 100 Coater and Bake Station***							
9	Resist Coat	AZ 1518	CEE Coat /Bake	1518 2.5K_CC-PRIME	2500 RPM, 60sec	Place the wafer on the spin chuck and then center then wafer. Once the wafer is centered, dispense resist until 50% of the wafer surface is covered, close the lid and start the spin program. When the program ends, open the lid of the CEE Coater, remove the wafer and place it on the hot plate.		
10	Soft Bake		CEE Coat /Bake	100C	100°C for 60sec	When baking is complete, remove the wafer and place on the table to cool. Two tweezers may be needed.		
11	Cool down		Grating next to hotplate		1min	Let wafer cool > 1 min before exposure		
12	***Expose and Develop***							
13	Load Mask Plate with Transparency		Karl Suss MA6 Contact Aligner			- matte ink side of transparency face UP (against wafer), glossy side of transparency should be touching glass plate - Tape the transparency to a 5-inch glass plate with narrow Kapton tape. - Kapton tape on corners only. Fold the tape ends. - Make sure tape doesn't go onto the back side of the plate!		
14	Expose		Karl Suss MA6 Contact Aligner	Hard Contact	Contact gap: 50 um **Example Exposure Time: 14.8 sec** **Calculate exposure time needed.**	Dose needed: **120 mJ/cm^2 (calculate exposure time)** Time (sec) = Dose (mJ) / Power (mW) 2024-01-05 lamp check: CH1, 6.43mw/cm2 thru plate+transparency		
15	Setup Develop	AZ 300MiF DI Water	Developer Wet Bench	150x75mm Developer beaker Larger "1st rinse" beaker Larger "2nd rinse" beaker/plastic container, final DI rinse in sink	Dev: AZ 300MIF DI water in both "rinse" beakers			
16	Develop	AZ 300MiF	Developer Wet Bench	Drop wafer into developer beaker, pour developer on top of wafer, push down with tweezers Agitate/swirl during develop (30sec)	Develop 30 sec			
17	Rinse	DI water Rinse #1	Developer Wet Bench	DI water beaker agitate/swirl 10sec		1st rinse liquid must be collected in benchtop container		
18	Rinse	DI water Rinse #2	Developer Wet Bench	DI water beaker agitate/swirl 10sec		2nd rinse liquid can be disposed down the drain		
19	N2 Dry		Developer Wet Bench	N2 gun	on absorbent wipe	use N2 to remove DI, make sure no developer remains		

20	***Buffered Oxide Etch (BOE) Etch***							
21	Load wafer into Cassette			Load all wafers into a single cassette	Make sure you can see the wafer underside easily.			
22	Oxide Etch (STAFF ONLY)	BHF + PPE	BOE Bath - Acid/Base Bench #3		Approx 2 min etch, then inspect	BOE is premixed 20:1 Ammonium fluoride:HF acid. HF (Hydrofluoric Acid) is used in this process. Safety is paramount. PPE is required. Perform according to Safety Orientation standards.		
23	After approx 30 sec, Inspect wafer underside	BHF + PPE	BOE Bath - Acid/Base Bench #3		Backside should be hydrophilic still			
24	Oxide Etch (STAFF ONLY)	BHF + PPE	BOE Bath - Acid/Base Bench #3		About 8 min more until the backside is hydrophilic (approx. 9 - 9.5 min). Start checking at ~7.5min. Remove when the backside is hydrophobic.	BOE is premixed 20:1 Ammonium fluoride:HF acid. HF (Hydrofluoric Acid) is used in this process. Safety is paramount. PPE is required. Perform according to Safety Orientation standards.		
25	Rinse #1	DI	Teflon beaker of DI	submerge wafer and remove	15 sec, check hydrophobicity			
26	Rinse #2	DI	Waterfall Bath- Acid/Base Bench #3	submerge wafers	additional 15 sec, continue until exposed Si is hydrophobic			
27	Rinse #3	DI	Waterfall Bath- Acid/Base Bench #3	spray into sink		final rinse with DI gun into sink (rinse thoroughly)		
28	N2 Dry		Developer Wet Bench	N2 gun	on absorbent wipe			
29	***Resist Strip***							
30	Resist Strip	Acetone beaker	Solvent Bench, directly into bench		10-20 sec, cover the whole wafer, don't let the wafer dry.	This stainless steel hood is metal due to the fact that solvents are often flammable		
31		IPA beaker	Solvent Bench, directly into bench		~10 sec cover whole wafer			
32		IPA squirt bottle	Solvent Bench, directly into bench	hold over same beaker	cover whole wafer			
33	N2 Dry	N2	Solvent Bench			take home your very own work of (wafer) art!		
34						**Art Wafer completed (Demo product): Instructor Initials**		

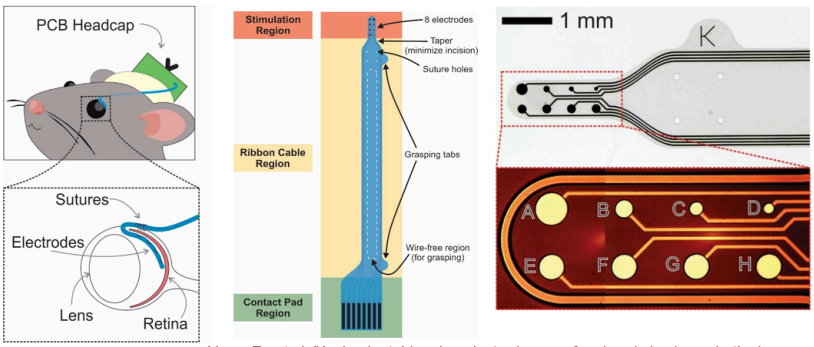
USC NanoLab
John O'Brien Nanofabrication Laboratory

USC Project: Microfabrication of Polyimide Microelectrode Arrays and Art Wafer

Bio MEMS – Neural Probe Implantation in retina

Dr. Eugene Yoon, Prof Ellis Meng

Fabrication of a microelectrode neural probe implantable on rat retina for partial restoration of visual function due to retinal diseases





Yoon, E., et al. "An implantable microelectrode array for chronic in vivo epiretinal stimulation of the rat retina." *Journal of Micromechanics and Microengineering* 30.12 (2020): 124001.

USC Viterbi School of Engineering | DREAMS Defense Ready Electronics and Microdevices Superhub | COMMONS | USC Viterbi John D. O'Brien Nanofabrication Laboratory | University of Southern California

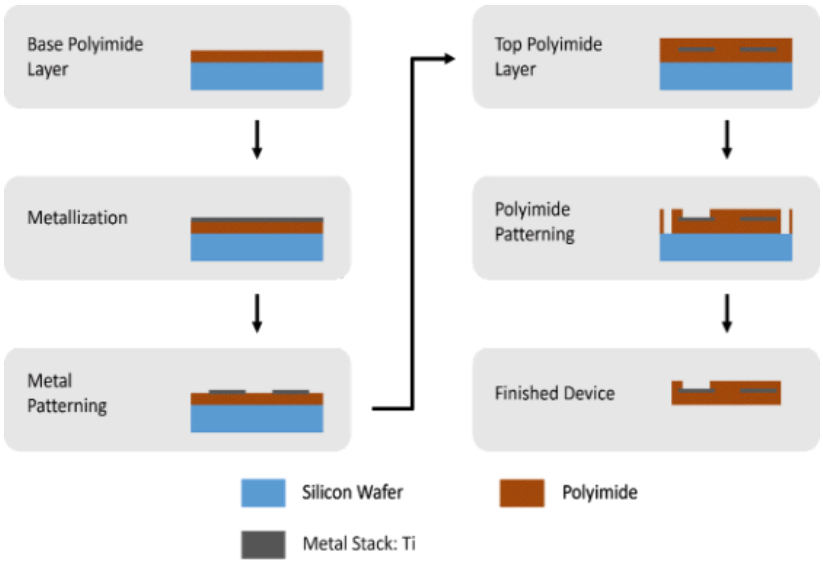
USC NanoLab John O'Brien Nanofabrication Laboratory	Neural Probe		Rev. 2024-09-03	Tracking Initials/ Date
Step	**Procedure**	**Tool**	**Parameters**	**Details**	**W1**
	Initial Wafers				
	Silicon Wafers, 4-inch Diameter, Single-Side Polished. Silicon Wafer thickness is 600 um.				
1	**Wafer Cleaning**				
2	Acetone Rinse	Solvent Wet Bench		Use Acetone squeeze bottle (red cap) to rinse wafer over empty beaker	
3	Isopropanol alcohol (IPA) Rinse	Solvent Wet Bench		Use IPA squeeze bottle (yellow cap) to rinse wafer over same beaker	
4	Nitrogen (N2) Dry	Solvent Wet Bench		Use N2 spray to dry wafer on Cleanroom Wipe. Dispose all solvent waste into the drain.	
5	Pre-Bake	Apogee Bake Plate	110°C for 5 m	Place wafer on Bake Plate set to 110°C for 5 m	
6	Cool Down	Cleanroom Wipe	1 m	Place wafer on Cleanroom Wipe next to Bake Plate to cool down for 1 m	
7	**Base Polyimide Layer**				
8	**1st Polyimide (PI) Curing**				
9	PI-2611 Dispense & Rest	Laurell Spin Coater	1 m	Center wafer onto spin chuck, spray N2, and turn on vacuum. Pour PI onto wafer to cover over 50% of wafer. Allow PI to rest for 1 m	

10	PI Spin Coat	Laurell Spin Coater	Spin coat 1st layer of ~5 µm of PI	Step 1: 10 s, 500 RPM, 500 RPM/s Step 2: 15 s, 1000 RPM, 500 RPM/s Step 3: 40 s, 2800 RPM, 500 RPM/s Allow PI to rest for 1 m	
11	Soft Bake	Apogee Bake Plate	85°C for 120 s 135°C for 120 s 165°C for 120 s	Set Bake Plate 1 to 85°C Set Bake Plate 2 to 135°C Set Bake Plate 4 to 165°C	
12	Hard Bake	Apogee Bake Plate	Recipe Name: PI Curing	Record wafer positions on Bake Plate 4. Run PI Curing recipe on Bake Plate 4. Allow wafers to cool overnight	
13	**Metalization**				
14	**1st Photolithography with Metal Mask**				
15	AZ 5214E-IR Resist Spin Coat	Laurell Spin Coater	3200 RPM 500 RPM/s 40s	Center wafer onto spin chuck, spray N2, and turn on vacuum. Use Pipette to dispense resist to cover 75% of wafer. Resist thickness is ~1.14 µm	
16	Soft Bake	Apogee Bake Plate	110°C for 60s		
17	**Expose**				
18	Initialize Mask Aligner and Measure Dose	Karl Suss MA/BA6 Mask Aligner		Initialize Mask Aligner and measure dose one time. Dose is automatically measured during start process step	
19	Load 1st Mask to Mask Holder	Karl Suss MA/BA6 Mask Aligner		Load and secure 1st Mask onto Mask Holder. Spray N2 on Mask. Load Mask Holder into aligner.	
20	Expose Wafer	Karl Suss MA/BA6 Mask Aligner	Hard Contact & 42.5 mJ/cm2 are settings in recipe	Use Recipe "Neural Probe Metal Mask 42.5 mJ-cm2." Load wafer onto aligner chuck and expose	
21	Image Reversal Bake	Apogee Bake Plate	110°C for 63s	Image Reversal Bake changes resist from Positive to Negative	
22	Cool Down	Cleanroom Wipe	3 m	Place wafer on Cleanroom Wipe to cool down for 3 m	
23	Remove Mask and Unplug Vacuum Line	Karl Suss MA/BA6 Mask Aligner		Remove Mask from the Mask Holder and unplug the Mask Vacuum line	
24	Flood Exposure	Karl Suss MA/BA6 Mask Aligner	291 mJ/cm2 is a setting in recipe	Use Recipe "Neural Probe Flood Exposure 291 mJ-cm2." Load wafer onto aligner chuck and expose	
25	Cool Down with Deionized Water (DI)	Developer Wet Bench	10 s	Prepare a beaker with 100 mL DI water and place wafer into beaker to prevent overheating	
26	**Develop**				
27	Prepare AZ 340 Developer	Developer Wet Bench		Prepare and label a beaker with 50 mL AZ 300 MIF Developer. Add 200 mL DI Water to developer to dilute to 1:4 ratio	
28	Develop with AZ 340 Developer	Developer Wet Bench	18 s	Fully submerge and gently agitate the wafer in developer for 18 s.	
29	1st DI Rinse	Developer Wet Bench	≥ 10 s	Transfer wafer to DI and agitate for ≥ 10 s. Dispose DI into the drain and dispose of the developer into the waste bottle.	
30	2nd DI Rinse	Developer Wet Bench	≥ 30 s	Rinse wafer with fresh DI for ≥ 30 s.	
31	N2 Dry	Developer Wet Bench		Place wafer on Cleanroom Wipe and use N2 spray to dry wafer	
32	Inspect	Nikon LV150 Microscope		Inspect wafer and ensure the exposed area has developed (uniform color). Compare to an underdeveloped wafer. If not, then develop for additional 10s. If features are not well defined, then proceed to re-work the wafer.	

33				**1st Photolithography Completed. Instructor initials:**	
34	**Metal Patterning**				
35	**Metal Deposition**				
36	Load wafers onto Substrate Holder of Deposition Tool	CHA Mark 40 E-Beam Evaporator		Load and record the position of each wafer in the Substrate Holder	
37	Staff only - Deposit Metals	CHA Mark 40 E-Beam Evaporator	Titanium (Ti) 100 nm @ 1.5 A/s	Staff will run one recipe to deposit 100 nm of Titanium	
38	Unload Wafers	CHA Mark 40 E-Beam Evaporator		Unload wafers from Substrate Holder	
39	**Metal Lift-Off**				
40	Prepare Ultrasonic (U/S) Bath	Solvent Wet Bench	80% Power Middle Frequency	Fill bath with DI Water Set power to 80% Select Middle Frequency	
41	Metal Lift-Off with Acetone	Solvent Wet Bench	2 m	Prepare and label Beaker filled to 1" depth with Acetone. Fully submerge the wafer in Acetone. Place Beaker in U/S Bath and sonicate for 2 m.	
42	Acetone Rinse	Solvent Wet Bench	30 s	Use an Acetone squeeze bottle (red cap) to rinse wafer for 30s over the same beaker.	
43	IPA Rinse	Solvent Wet Bench	30 s	Use IPA squeeze bottle (yellow cap) to rinse wafer for 30s over same beaker	
44	N2 Dry	Solvent Wet Bench		Place wafer on Cleanroom Wipe and use N2 spray to dry wafer. Dispose all solvent waste into the drain.	
45	Inspect	Solvent Wet Bench		Inspect the wafer and ensure that metal has lifted off. Repeat sonication if less than 50% of devices are clean.	
46				**Deposition and Lift-Off completed. Instructor initials:**	
47	**Top Polyimide Layer**				
48	**2nd Polyimide (PI) Curing**				
49	PI-2611 Dispense & Rest	Laurell Spin Coater	1 m	Center wafer onto spin chuck, spray N2, and turn on vacuum. Pour PI onto wafer to cover over 50% of wafer. Allow PI to rest for 1 m	
50	PI Spin Coat	Laurell Spin Coater	Spin coat 2nd layer of ~5 µm of PI	Step 1: 10 s, 500 RPM, 500 RPM/s Step 2: 15 s, 1000 RPM, 500 RPM/s Step 3: 40 s, 2800 RPM, 500 RPM/s Allow PI to rest for 1 m	
51	Soft Bake	Apogee Bake Plate	85°C for 120 s 135°C for 120 s 165°C for 120 s	Set Bake Plate 1 to 85°C Set Bake Plate 2 to 135°C Set Bake Plate 4 to 165°C	
52	Hard Bake	Apogee Bake Plate	Recipe Name: PI Curing	Record wafer positions on Bake Plate 4. Run PI Curing recipe on Bake Plate 4. Allow wafers to cool overnight	
53	**Polyimide Patterning**				
54	**2nd Photolithography with Etch Mask**				
55	Pre-Bake	Apogee Bake Plate	135°C for 5 m	Place wafer on Bake Plate set to 135°C for 5 m	
56	Cool Down	Cleanroom Wipe	1 m	Place wafer on Cleanroom Wipe next to Bake Plate to cool down for 1 m	
57	AZ P4620 Resist Spin Coat	Laurell Spin Coater	1000 RPM 500 RPM/s 45s	Center wafer onto spin chuck, spray N2, and turn on vacuum. Use Pipette to dispense resist to cover 75% of wafer. Resist thickness is ~15 µm	

58	Soft Bake	Apogee Bake Plate	115°C for 4 m		
59	Rehydration	Wafer Cassette Box	15 m at 50% Humidity	Dampen a cleanroom wipe with DI and place it into the Wafer Cassette Box. Place Wafers into a cassette box for 15 m.	
60	**Expose**				
61	Initialize Mask Aligner and Measure Dose	Karl Suss MA/BA6 Mask Aligner		Initialize Mask Aligner and measure dose one time. Dose is automatically measured during start process step	
62	Load 1st Mask to Mask Holder	Karl Suss MA/BA6 Mask Aligner		Load and secure 1st Mask onto Mask Holder. Spray N2 on Mask. Load Mask Holder into aligner.	
63	Expose Wafer	Karl Suss MA/BA6 Mask Aligner	Soft Contact & 550 mJ/cm2 are settings in recipe	Use Recipe "Neural Probe Etch Mask 550 mJ-cm2." Load wafer onto aligner chuck and expose	
64	Cool Down with Deionized Water (DI)	Developer Wet Bench	2 m	Prepare a beaker with 100 mL DI water and place wafer into beaker to prevent overheating	
65	**Develop**				
66	Prepare AZ 340 Developer	Developer Wet Bench		Prepare and label a beaker with 50 mL AZ 300 MIF Developer. Add 200 mL DI Water to developer to dilute to 1:4 ratio	
67	Develop with AZ 340 Developer	Developer Wet Bench	300 s	Fully submerge and gently agitate the wafer in developer for 300 s.	
68	1st DI Rinse	Developer Wet Bench	≥ 10 s	Transfer wafer to DI and agitate for ≥ 10 s. Dispose DI into drain and dispose developer into waste bottle.	
69	2nd DI Rinse	Developer Wet Bench	≥ 30 s	Rinse wafer with fresh DI for ≥ 30 s.	
70	N2 Dry	Developer Wet Bench		Place wafer on Cleanroom Wipe and use N2 spray to dry wafer	
71	Inspect	Nikon LV150 Microscope		Inspect wafer and ensure the exposed area has developed (uniform color). Compare to an underdeveloped wafer. If not, then develop for additional 10s. If features are not well defined, then proceed to re-work the wafer.	
72				**2nd Photolithography Completed. Instructor initials:**	
73	**Polyimide Etch**				
74	Edge Bead Removal	Etch Bay Fumehood		Use an Acetone squeeze bottle to soak two cleanroom swabs. Remove edge bead resist at the edge of wafers	
75	1st Plasma Etch	Oxford Deep Reactive-Ion Etcher (DRIE)	40 cycles is set in the recipe and etch rate is 0.6 - 0.8 µm/m	Load Wafer into Dry Etcher load lock and pump to Base Pressure. Run Recipe “Polyimide Meng Lab V1.”	
76	2nd Plasma Etch	Oxford Deep Reactive-Ion Etcher (DRIE)	Repeat above recipe for a total of 80 cycles	After the 1st run, leave the wafer in Load Lock. Repeat Recipe “Polyimide Meng Lab V1.”	
77	**Finished Device**				
78	**Release Neural Probes**				
79	Acetone Rinse	Solvent Wet Bench	30 s	Prepare and label Beaker filled to 1" depth with Acetone. Fully submerge the wafer in Acetone. Place Beaker in U/S Bath and sonicate for 30 s.	
80	Acetone Rinse	Solvent Wet Bench	10 s	Use an Acetone squeeze bottle (red cap) to rinse wafer for 10 s over the same beaker.	
81	IPA Rinse	Solvent Wet Bench	30 s	Use IPA squeeze bottle (yellow cap) to rinse wafer for 30 s over same beaker	

82	N2 Dry	Solvent Wet Bench		Place wafer on Cleanroom Wipe and use N2 spray to dry wafer. Dispose all solvent waste into the drain.	
83	DI Soak	Solvent Wet Bench		Use DI squeeze bottle to soak devices with DI water.	
84	Release Neural Probes	Solvent Wet Bench		Use tweezers to lift the edge of devices at the thin end and slowly pull up the entire probe.	
85				**Device Release Completed. Instructor initials:**	



USC NanoLab
John O'Brien Nanofabrication Laboratory

USC Project: Art Wafer

USC NanoLab John O'Brien Nanofabrication Laboratory	Art Wafer		Rev. 2024-08-26	Tracking Initials/ Date
Step	**Procedure**	**Tool**	**Parameters**	**Details**	**W1**
	Initial Wafers				
	Silicon Wafers, 3-inch Diameter, Single-Side Polished with 560 nm of Silicon Dioxide coated on one side. Silicon Wafer thickness is 381 um.				
1	**Wafer Cleaning**				
2	Acetone Rinse	Solvent Wet Bench		Use Acetone squeeze bottle (red cap) to rinse wafer	
3	Isopropanol alcohol (IPA) Rinse	Solvent Wet Bench		Use IPA squeeze bottle (yellow cap) to rinse wafer	
4	Nitrogen (N2) Dry	Solvent Wet Bench		Place wafer on Cleanroom Wipe and use N2 spray to dry wafer	
5	Pre-Bake	Apogee Bake Plate	100°C for 30s	Place wafer on Bake Plate set to 100°C for 30s	
6	**Hexamethyldisilazane Spin Coat**				
7	Hexamethyldisilazane (HMDS) Primer Spin	Laurell Spin Coater	10s soak 3000 RPM 500 RPM/s 60s	Center wafer onto spin chuck, spray N2, and turn on vacuum. Use Pipette to dispense HMDS to cover 75% of wafer.	
8	HMDS Primer Bake	Apogee Bake Plate	100°C for 60s	Place wafer on Bake Plate set to 100°C for 60s	
10	Cool Down	Cleanroom Wipe	1 m	Place wafer on Cleanroom Wipe next to Bake Plate to cool down for 1 m	
11	IPA Wipe Down (needed if using same spin coater for resist)	Laurell Spin Coater		Dampen Cleanroom Wipe with IPA and wipe down Spin Coater	
12	**Resist Spin Coat**				
13	AZ 1518 Resist Spin Coat	Laurell Spin Coater	2500 RPM 500 RPM/s 60s	Center wafer onto spin chuck, spray N2, and turn on vacuum. Use Pipette to dispense resist to cover 75% of wafer.	
14	Soft Bake	Apogee Bake Plate	100°C for 60s		
15	**Expose**				
16	Measure Mask Aligner Intensity	Karl Suss MJB3 Mask Aligner	Record Intensity:	Measure intensity of Mask Aligner with UV Meter one time.	
17	Create Mask			Spray N2 on transparency. Create a mask by using Kapton tape to secure corners of transparency to the glass sheet.	
18	Load Mask and Mask Holder	Karl Suss MJB3 Mask Aligner		Load Mask onto Mask Holder and press the Vacuum button. Spray N2 on Mask. Load Mask Holder into aligner.	
19	Expose Wafer	Karl Suss MJB3 Mask Aligner	Calculate Exposure Time needed for 120 mJ/cm^2:	Load Wafer onto an aligner chuck, adjust timer, and expose with Soft Contact.	
	Develop				

20	Prepare AZ 300 MIF Developer	Developer Wet Bench		Prepare and label a beaker with 100 mL AZ 300 MIF Developer. Prepare and label a beaker with 100 mL Deionized (DI) Water.	
21	Develop with AZ 300 MIF Developer	Developer Wet Bench		Fully submerge wafer into developer for 30s.	
22	1st DI Rinse	Developer Wet Bench		Transfer wafer to DI and agitate for ≥10s. Dispose DI rinse into drain and dispose developer into waste bottle.	
23	2nd DI Rinse	Developer Wet Bench		Rinse wafer with fresh DI for ≥30s.	
24	N2 Dry	Developer Wet Bench		Place wafer on Cleanroom Wipe and use N2 spray to dry wafer	
25	Load Wafer into Cassette	Etch Bay		Load all wafers into a single cassette	
26	Staff only - Buffered Oxide Etch (BOE)	Acid Wet Bench		Staff will equip PPE and etch wafers with premixed BOE 20:1 in Teflon beaker for 60s	
27	Staff only - 1st DI Rinse	Acid Wet Bench		Staff will transfer wafer to DI and agitate for ≥10s. Dispose DI into the drain and BOE into the waste bottle.	
28	Staff only - 2nd DI Rinse	Acid Wet Bench		Rinse wafer with fresh DI for ≥30s and return wafers	
29	N2 Dry	Developer Wet Bench		Place wafer on Cleanroom Wipe and use N2 spray to dry wafer	
30	**Resist Strip**				
31	Resist strip with Acetone	Solvent Wet Bench		Prepare and Label Beaker with 100 - 200 mL Acetone.Fully submerge wafer in Acetone for 10 - 20s	
32	IPA Rinse	Solvent Wet Bench		Prepare and Label Beaker with 100 - 200 mL IPA. Fully submerge wafer in IPA for 10 - 20s	
33	IPA Rinse	Solvent Wet Bench		Use Tweezers to pick up wafer and rinse wafer with IPA squeeze bottle	
34	N2 Dry	Solvent Wet Bench		Place wafer on Cleanroom Wipe and use N2 spray to dry wafer. Dispose all solvent waste into the drain.	
35				**Art Wafer Completed (Demo Product). Instructor initials:**	

USC Project: Micro-Pressure Sensor

USC NanoLab John O'Brien Nanofabrication Laboratory	Pressure Sensor		Rev. 2024-11-27	Tracking Initials/ Date
Step	**Procedure**	**Tool**	**Parameters**	**Details**	**W1**
	Initial Wafers				
	Silicon Wafers, 3-inch Diameter, Single-Side Polished with 1000 nm of Silicon Nitride coating on both sides. Silicon Wafer thickness is 380 um.				
1	**Wafer Cleaning**				
2	Acetone Rinse	Solvent Wet Bench		Use Acetone squeeze bottle (red cap) to rinse wafer over empty beaker.	
3	Isopropanol alcohol (IPA) Rinse	Solvent Wet Bench		Use IPA squeeze bottle (yellow cap) to rinse wafer over same beaker.	
4	Nitrogen (N2) Dry	Solvent Wet Bench		Use N2 spray to dry wafer on Cleanroom Wipe. Dispose all solvent waste into the drain.	
5	Pre-Bake	Apogee Bake Plate	100°C for 30s	Place wafer on a Bake Plate set to 100°C for 30s.	
6	**Hexamethyldisilazane Spin Coat**				
7	Hexamethyldisilazane (HMDS) Primer Spin	Laurell Spin Coater	10s soak 3000 RPM 500 RPM/s 60 s	Center wafer onto spin chuck, spray N2, and turn on vacuum. Use Pipette to dispense HMDS to cover 75% of wafer.	
8	HMDS Primer Bake	Apogee Bake Plate	100°C for 60 s	Place wafer on a Bake Plate set to 100°C for 60 s.	
9	Cool Down	Cleanroom Wipe	1 m	Place wafer on the Cleanroom Wipe next to the Bake Plate to cool down for 1 m.	
10	IPA Wipe Down (needed if using same spin coater for resist)	Laurell Spin Coater		Dampen Cleanroom Wipe with IPA and wipe down Spin Coater.	
11	**Front Side - Wheat Stone Bridge Metal Resistors**				
12	**Resist Spin Coat**				
13	AZ 1518 Resist Spin Coat	Laurell Spin Coater	2500 RPM 500 RPM/s 60 s	Center wafer onto spin chuck, spray N2, and turn on vacuum. Use Pipette to dispense resist to cover 75% of wafer.	
14	Soft Bake	Apogee Bake Plate	100°C for 60 s		
15	**Expose**				
16	Initialize Mask Aligner and Measure Dose	Karl Suss MA/BA6 Mask Aligner		Initialize Mask Aligner and measure dose one time. Dose is automatically measured during start process step	
17	Load 1st (Front Side) Mask to Mask Holder	Karl Suss MA/BA6 Mask Aligner		Load and secure 1st Mask onto Mask Holder. Spray N2 on Mask. Load Mask Holder into aligner.	
18	Expose Wafer	Karl Suss MA/BA6 Mask Aligner	Soft Contact, 20um gap, & 136 mJ/cm^2 are settings in recipe	Load wafer onto aligner chuck and expose.	
19	Cool Down	Cleanroom Wipe	1 m	Place wafer on the Cleanroom Wipe next to the Bake Plate to cool down for 1 m.	

20	**Develop**				
21	Prepare AZ 300 MIF Developer	Developer Wet Bench		Prepare and label a beaker with 100 mL AZ 300 MIF Developer. Prepare and label a beaker with 100 mL Deionized (DI) Water.	
22	Develop with AZ 300 MIF Developer	Developer Wet Bench	60 s	Fully submerge and gently agitate the wafer in developer for 60 s.	
23	1st DI Rinse	Developer Wet Bench	≥ 10 s	Transfer wafer to DI and agitate for ≥ 10 s. Dispose DI into drain and dispose developer into waste bottle.	
24	2nd DI Rinse	Developer Wet Bench	≥ 30 s	Rinse wafer with fresh DI for ≥ 30 s.	
25	N2 Dry	Developer Wet Bench		Place wafer on Cleanroom Wipe and use N2 spray to dry wafer.	
26	Inspect	Nikon LV150 Microscope		Inspect wafer and ensure the exposed area has developed (uniform color). Compare to an underdeveloped wafer. If not, then develop for additional 10 s. If features are not well defined, then proceed to re-work the wafer.	
27				**Front Side Photolithography completed. Instructor initials:**	
28	**Re-work Wafer (if needed)**				
29	Resist strip with Acetone	Solvent Wet Bench	30 s	Prepare and Label Beaker with 100 - 200 mL Acetone.Fully submerge wafer in Acetone for 30s.	
30	IPA Rinse	Solvent Wet Bench	30 s	Prepare and Label Beaker with 100 - 200 mL IPA.Fully submerge wafer in IPA for 30s.	
31	IPA Rinse	Solvent Wet Bench	5 - 10 s	Use Tweezers to pick up the wafer and rinse the wafer with an IPA squeeze bottle.	
32	N2 Dry	Solvent Wet Bench		Place wafer on Cleanroom Wipe and use N2 spray to dry wafer. Dispose all solvent waste into the drain.	
33	Pre-Bake	Apogee Bake Plate	110°C for 30 s	Place wafer on a Bake Plate set to 110°C for 30 s.	
34	Restart Photolithography Steps			Repeat HMDS Spin Coat steps, Resist Spin Coat steps, Expose steps, and Develop Steps.	
35	**Metal Deposition**				
36	Load wafers onto Substate Holder of Deposition Tool	CHA Mark 40 E-Beam Evaporator		Load and record the position of each wafer in the Substrate Holder.	
37	Staff only - Deposit Metals	CHA Mark 40 E-Beam Evaporator	Chromium (Cr) 30 Å @ 1 Å/s Gold (Au): 1000 Å @ 2 Å/s	Staff will run two recipes to deposit one Chromium adhesion layer and one Gold layer.	
38	Unload Wafers	CHA Mark 40 E-Beam Evaporator		Unload wafers from Substrate Holder.	
39	**Metal Lift-Off**				
40	Prepare Ultrasonic (U/S) Bath	Solvent Wet Bench	80% Power Middle Frequency	Fill bath with DI Water Set power to 80% Select Middle Frequency	

27				**Front Side Photolithography completed. Instructor initials:**	
41	Metal Lift-Off with Acetone	Solvent Wet Bench	2 m	Prepare and Label Beaker filled to 1" depth with Acetone. Fully submerge wafer in Acetone. Place Beaker in U/S Bath and sonicate for 2 m.	
42	Acetone Rinse	Solvent Wet Bench	30 s	Use Acetone squeeze bottle (red cap) to rinse wafer for 30s over the same beaker.	
43	IPA Rinse	Solvent Wet Bench	30 s	Use IPA squeeze bottle (yellow cap) to rinse wafer for 30s over the same beaker.	
44	N2 Dry	Solvent Wet Bench		Place wafer on Cleanroom Wipe and use N2 spray to dry wafer. Dispose all solvent waste into the drain.	
45	Inspect	Nikon LV150 Microscope		Inspect wafer and ensure that metal has lifted off around the wheatstone bridge circuit. Repeat sonication if less than 50% of devices are clean.	
46				**Deposition and Lift-Off completed. Instructor initials:**	
47	**Front Side Spin Coat - Thick Resist as Protection Layer**				
48	HMDS Primer Spin	Laurell Spin Coater	10s soak 3000 RPM 500 RPM/s 60 s	Center wafer onto spin chuck, spray N2, and turn on vacuum. Use Pipette to dispense HMDS to cover 75% of wafer.	
49	HMDS Primer Bake	Apogee Bake Plate	100°C for 60s	Place wafer on a Bake Plate set to 100°C for 60s.	
50	Cool Down	Cleanroom Wipe	1 m	Place wafer on the Cleanroom Wipe next to the Bake Plate to cool down for 1 m.	
51	IPA Wipe Down (needed if using same spin coater for resist)	Laurell Spin Coater		Dampen Cleanroom Wipe with IPA and wipe down Spin Coater.	
52	AZ 1518 Resist Spin Coat	Laurell Spin Coater	1000 RPM 500 RPM/s 60 s	Center wafer onto spin chuck, spray N2, and turn on vacuum. Use Pipette to dispense resist to cover 75% of wafer.	
53	Soft Bake	Apogee Bake Plate	100°C for 120s		
54	Cool Down	Cleanroom Wipe	1 m	Place wafer on the Cleanroom Wipe next to the Bake Plate to cool down for 1 m.	
55	**Back Side - Membrane Window**				
56	**Resist Spin Coat - Back Side**				
57	HMDS Primer Spin	Laurell Spin Coater	10s soak 3000 RPM 500 RPM/s 60 s	Center wafer onto spin chuck, spray N2, and turn on vacuum. Use Pipette to dispense HMDS to cover 75% of wafer.	
58	HMDS Primer Bake	Apogee Bake Plate	100°C for 60 s	Place wafer on a Bake Plate set to 100°C for 60 s.	
59	Cool Down	Cleanroom Wipe	1 m	Place wafer on the Cleanroom Wipe next to the Bake Plate to cool down for 1 m.	
60	IPA Wipe Down (needed if using same spin coater for resist)	Laurell Spin Coater		Dampen Cleanroom Wipe with IPA and wipe down Spin Coater.	
61	AZ 1518 Resist Spin Coat	Laurell Spin Coater	1000 RPM 500 RPM/s 60 s	Center wafer onto spin chuck, spray N2, and turn on vacuum. Use Pipette to dispense resist to cover 75% of wafer.	
62	Soft Bake	Apogee Bake Plate	100°C for 120s		
63	Cool Down	Cleanroom Wipe	1 m	Place wafer on the Cleanroom Wipe next to the Bake Plate to cool down for 1 m.	
64	**Expose - Back Side**				

65	Initialize Mask Aligner and Measure Dose	Karl Suss MA/BA6 Mask Aligner		Initialize Mask Aligner and measure dose one time. Dose is automatically measured during the start process step.	
66	Set up(Back Side) Mask to Mask Holder	Karl Suss MA/BA6 Mask Aligner		Load and secure 2nd Mask onto Mask Holder. Spray N2 on Mask. Load Mask Holder into aligner.	
67	Expose Wafer	Karl Suss MA/BA6 Mask Aligner	50um Expose Gap & 550 mJ/cm^2 are settings in recipe	Load and expose wafer using Back Side Alignment (BSA) procedures.	
68	**Develop - Back Side**				
69	Prepare AZ 300 MIF Developer	Developer Wet Bench		Prepare and label a beaker with 100 mL AZ 300 MIF Developer. Prepare and label a beaker with 100 mL Deionized (DI) Water.	
70	Develop with AZ 300 MIF Developer	Developer Wet Bench	120 s	Fully submerge and gently agitate wafer in developer for 120s.	
71	1st DI Rinse	Developer Wet Bench	≥ 10 s	Transfer wafer to DI and agitate for ≥ 10 s. Dispose DI into drain and dispose developer into waste bottle.	
72	2nd DI Rinse	Developer Wet Bench	≥ 30 s	Rinse wafer with fresh DI for ≥ 30 s.	
73	N2 Dry	Developer Wet Bench		Place wafer on Cleanroom Wipe and use N2 spray to dry wafer.	
74	Inspect	Nikon LV150 Microscope		Inspect wafer and ensure the exposed area has developed (uniform color). Compare to an underdeveloped wafer. If not, then develop for additional 10s. If features are not well defined, then re-work is needed.	
75	**Nitride Dry Etch - Back Side**				
76	1st Plasma Etch	Oxford RIE 80	10 m	Load wafer with Back Side pattern facing up to Etch Silicon Nitride layer in Membrane Window.	
77	Visual Inspect			Visually inspect to see if there is color in the Member Windows due to partial etching.	
78	Rotate wafers 180°	Oxford RIE 80		Rotating wafers will ensure etch is uniform. Etch rate is slightly higher in the center.	
79	2nd Plasma Etch	Oxford RIE 80	10 m		
80	Visual Inspect			Visually inspect if Silicon Nitride is etched. Color should be uniform silicon-grey in the windows.	
81	Resist strip with Acetone	Solvent Wet Bench	1 m	Prepare and Label Beaker with 100 - 200 mL Acetone.Fully submerge wafer in Acetone for 1 m.	
82	IPA Rinse	Solvent Wet Bench		Use IPA squeeze bottle (yellow cap) to rinse wafer for 30s.	
83	N2 Dry	Solvent Wet Bench		Place wafer on Cleanroom Wipe and use N2 spray to dry wafer. Dispose all solvent waste into the drain.	
84				**Dry Etch Completed. Instructor initials:**	
85	**Membrane Release**				
86	**Pressure Sensor Cavity - Silicon Wet Etch**				

87	Prepare Potassium Hydroxie (KOH) Bath - Staff only	Developer Wet Bench		Fill Glass Beaker with KOH to 4" depth. Prepare and label a beaker with DI filled to 4" depth.	
88	Heat KOH Bath - Staff only	Developer Wet Bench	100°C - 130°C Setpoint	Place Glass Beaker on hotplate and set temperature to 100°C. Increase temperature as needed to stabilize KOH temperature at 90°C.	
89	KOH Etch - Staff only	Developer Wet Bench	90°C for 5 h	Load wafers onto dippers. Record position of each wafer. Place dipper + wafers into KOH bath for 5 hours.	
90	DI Rinse - Staff only	Developer Wet Bench	≥ 30 s	Transfer dipper + wafer to DI beaker for 30 s. Dispose DI into drain and dispose developer into waste bottle.	
91	Waterfall DI Rinse - Staff only	Developer Wet Bench	≥ 30 s	Slightly open DI faucet valve to dispense at low pressure. Rinse dipper + wafers with DI from faucet for 60 s.	
92	Overnight Drying - Staff only	Developer Wet Bench		Allow dipper + wafers to dry overnight on Cleanroom Wipe	
93	Distribute wafers - Staff only	Developer Wet Bench		Staff will distribute etched wafers. Care must be taken as wafers are more fragile post-KOH etch	
94				**Wet Etch Completed. Instructor initials:**	

Implementing your own fabrication project:

If your cleanroom already has fabrication projects that may be easy to implement as trainer projects, here are the key steps for ensuring the project still meets the requirements for IEEE Microcredentials while encouraging increased participation in the semiconductor industry.

A. Plan for your participants to learn your cleanroom's safety fundamentals *online* before the Gateway cohort begins, and *pass* (eg. >70%) an open-book online safety quiz about that material (multiple tries are acceptable). Your participants will be supervised by expert staff/TA's the whole time, so the purpose of this is to ensure they learn the fundamentals and pay attention during the cohort.
B. In addition to the safety quiz, have students fill our demographics/survey information, photo release forms, liability waivers etc. during onboarding (online, eg. a Canvas page).
C. Train and retrain your TA's and staff to require participants to find answers on their process travelers, instead of telling participants what to do. Require participants to initial/write comments+updates on their Process Traveler at every step. Industry has stated that these experiences are key outcomes for "Cleanroom Protocols" credentials.

D. Ensure you print out well-written and easy to follow (a) process travelers/Run-Cards, and (b) Operating procedures for all relevant equipment. (meets the “Cleanroom Protocols” microcredential.)
E. Have staff or TA’s run a dry-run of the project to (a) train the TA’s, and (b) test all necessary equipment, and (c) identify missing procedures or variables in the process.
F. Get participants into the cleanroom on Day-1 if possible; the Art Wafer is a great project to start on Day 1, see below for more info.
G. Plan for ~3 days max of fabrication on the primary project. ~10 participants will take 3-4x longer than an experienced cleanroom user. This leaves time for other experiential learning, such as gowning, safety, metrology and other immersive fabrication tasks.
H. Utilize motivated and expert graduate-student users of your cleanroom as Teaching Assistants (TA’s) where possible. Choose TA’s that know the lab, equipment and are excited to teach.
I. Identify bottlenecks (such as single-wafer loading machines with long etch times), and redesign the process to utilize parallel or multi-wafer tools/steps. Run long steps overnight (with TA or staff help) when possible. This is important to minimize participant wait times during the course.
J. An “ArtWafer” is an excellent “introductory” short fabrication project to run on day 1. Students provide a photo of their own choosing, which will be “printed” via photolithography onto a silicon wafer (using direct-write or laser-printed transparencies), which students get to take home with them. This activity dramatically increases student engagement on Day 1. (Concept and implementation details courtesy Prof. Matt Pleil, Univ. of New Mexico).
K. If possible, you can simulate a night-shift “passdown” by having graduate-student TA’s perform a step overnight (for example, removing wafers from overnight chemical, or depositing all wafers overnight, after which the TA emails all participants with the “passdown” and/or verbally gives the passdown the next morning. Participants then update their travelers accordingly and proceed with the process the next day. This is a common practice in industrial manufacturing environments.